Subject: DE

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| **Lesson Plan Duration : Aug 2025 –Nov. 2025 work Load (Lecture/ Practical) per week (in hours): 03 hours (Theory) + 08 hours (04 Hours\*2 Groups) (PRACTICAL)** |
| **Name of the Faculty:** Sh. Alok Kumar **Discipline:** Electronics&CommunicationEngg**/**Computer Engg**. Subject:** DE **Semester:** 3rd |
| **Wee k** | **Theory** | **Practical** | **Week** | **Theory** | **Practical** |
| **Lecture day** | **Topic (including assignment/ test)** | **Topic** | **Lecture day** | **Topic (including assignment/ test)** | **Topic** |
|  |  | Unit 1. Introduction to | Verification and interpretation of truth tables for AND, OR, NOT NAND,NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gate |  |  | Operation using | Verification of |
|  | **1** | analog and digital signal |  | **22** | waveforms and truthtables of RS, T, D, | truth table forMultiplexers |
|  |  |  |  |  | Master/Slave JK flip | and x and De- |
| **1st** |  |  | **8th** |  | flops | Multiplexers |
| **2** | Binary, octal and hexadecimal number system | **23** | Difference between a latch and a flip flop |
|  |  | Conversions of number |  |  | Introduction and basic |  |
|  | **3** | systems |  | **24** | concepts including shift left and shift right |  |
| **2nd** | **4** | Binary addition and subtraction including binary points | Realisation of logic functions with the help of NAND or NOR gates | **9th** | **25** | Serial in parallel out, serial in serial out, parallel in serial out, parallel in parallel out,Universal shift register | To design a 4 bit SISO, SIPO, PISO,PIPO shift registers usingJK/D flip |
|  | 1’s and 2’s complement |  | Assignment 2 |
|  | **5** | method |  |  | **26** |  | flops and |
|  |  | of addition/subtraction. |  |  |  |  | verification of |
|  |  |  | their |
|  | Concept of code, |  | 2nd Sessional test |
|  | **6** | weighted and non- |  |  | **27** |  | operation. |
|  |  | weighted codes |  |  |  |  |  |
|  |  | 8421, BCD, excess-3 and | To design a half adder using XOR and NAND gates and verification of its operation |  |  | Unit 5. Working | To design a 4 |
|  | **7** | Gray code |  | **28** | principle of A/D and D/Aconverters, Stair step | bit ringcounter and |
|  |  |  |  |  | Ramp A/D converter | verify its |
| **3rd** |  |  | **10th** |  |  | operation |
|  | Concept of parity, single |  | Dual Slope A/D |
|  | **8** | and double parity and |  | **29** | converter |  |
|  |  | error detection |  |  |  |  |
|  |  | Unit 2. Concept of |  |  | Successive |  |
|  | **9** | negative and positive |  | **30** | Approximation A/D |  |
|  |  | logic |  |  | Converter |  |
|  |  | Definition, symbols and | To design of a full adder circuit using XOR and NAND gates and verify its operation |  |  | Binary Weighted D/A | Use of |
|  |  | truth tables of NOT, |  |  | converter | Asynchronous |
| **4th** | **10** | AND, OR, NAND, NOR, EXOR Gates, NAND | **11th** | **31** |  | Counter ICs (7490 or |
|  |  | and NOR as universal |  |  |  | 7493) |
| **11** | Introduction to TTL and | **32** | R/2R ladder D/A |
|  | CMOS logic families |  | converter |  |

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|  | **12** | Postulates of Booleanalgebra, De Morgan’s Theorems |  |  | **33** | Applications of A/D and D/A converter |  |
| **5th** | **13** | Karnaugh map (upto 4 variables), simple application in developingcombinational | To design circuit for 7 segment display ICs | **12th** | **34** | Memory organization, classification of semiconductor memories | To design and verification of A/D converter |
| **14** | Assignment 1 | **35** | Static and dynamic RAM |
| **15** | 1st sessional exam | **36** | Introduction to 74181ALU IC |
|  |  | Unit 3. Half adder, full | Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch, D flip- flop, JK flip- |  |  | Assignment 3 | To design and |
|  | **16** | adder design and |  | **37** |  | verification of |
|  |  | implementation |  |  |  | D/A converter |
| **17** | 4 bit adder circuit | **38** | Revision of chapter 5 |
| **6th** |  | Four bit decoder circuits | **13th** |  | 3rd sessional test |  |
|  |  | for 7 segment display and |  |  |  |  |
|  | **18** | decoder/driver Ics |  | **39** |  |  |
| **7th** | **19** | Basic functions and block diagram of MUX. DMUX | Verification of truth table for encoder and decoder ICs | **14th** | **40** | Revision of chapter 1 and chapter 2 | To design and verification of 74181 ALU IC |
| **20** | Basic functions and block diagram of Encoder | **41** | Revision of chapter 3 and chapter 4 |
|  |  | Unit 4. Concept and types |  |  |  | Revision of chapter 5 |  |
|  | **21** | of latch with their working and applications |  |  | **42** |  |  |